CLAIMS

1. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell block including a plurality of transistors formed in series on the semiconductor substrate, the memory transistors having first and second impurity-diffused regions and gates formed respectively between the first and second impurity-diffused regions and being connected in series, a plurality of memory cells each having a lower electrode connected to the first impurity-diffused region, a ferroelectric film formed on the lower electrode, and a first upper electrode formed on the ferroelectric film and being connected to the second impurity-diffused region; and

a block selecting transistor formed on the semiconductor substrate and being connected to one end of the memory cell block;

a second upper electrode formed adjoined to the block selecting transistor and being disconnected from the first upper electrode of the memory cell.

2. A semiconductor memory device according to claim 1, wherein the second upper electrode is formed on the ferroelectric film on the lower electrode.

3. A semiconductor memory device according to claim 1, wherein a distance between the second upper electrode and the first upper electrode formed adjacent to the block selecting transistor in the memory cells is equal to a distance between the first upper each electrode formed on the same lower electrode in the neighboring memory cells in the memory cell blocks.

4. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of memory transistor units formed on the semiconductor substrate and including a plurality of memory transistors having first and second impurity-diffused regions and a gate formed between the first and second impurity-diffused regions and being connected in series;

a plurality of plug electrodes respectively connected to one of the first impurity-diffused regions;

a block selecting transistor formed on the semiconductor substrate and adjoined to one memory transistor in one end of the memory transistor units, and having impurity-diffused regions and a gate;

a first wiring connected to the second impurity-diffused region in one end of the memory transistor units;

a lower electrode connected to the plug electrode connected to the first impurity-diffused region of the memory transistor in one end of the memory cell block;

a ferroelectric film formed on the lower electrode;

a first upper electrode formed on the ferroelectric film and being connected to the first wiring;

a second upper electrode formed on the ferroelectric film and being disconnected from the memory transistor, the plug electrode, the block selecting transistor and the first wiring; and

an insulating film formed over the semiconductor substrate, the memory transistors, the plug electrode, the first and second upper electrodes, the ferroelectric film, and the lower electrode.

5. A semiconductor memory according to claim 4, wherein the first upper electrode is formed above the gate of the memory transistor and the second upper electrode is formed

above the gate of the block selecting transistor.

6. A semiconductor memory device comprising:

a semiconductor substrate;

a memory transistor formed on the semiconductor substrate, and having first and second impurity-diffused regions and a gate;

a plug electrode connected to the first impurity-diffused region;

a first wiring connected to the second impurity-diffused region of the memory transistor;

a lower electrode connected to the plug electrode;

a ferroelectric film formed on the lower electrode;

a first upper electrode formed on the ferroelectric film and being connected to the first wiring;

a second upper electrode formed on the ferroelectric film and being disconnected from the memory transistor, the plug electrode, and the first wiring; and

an insulating film formed over the semiconductor substrate, the memory transistor, the plug electrode, the first and second upper electrode, the ferroelectric film and the lower electrode.

7. A semiconductor memory device according to claim 6, further comprising a plate line electrode formed on the first impurity-diffused region.

8. A semiconductor memory device according to claim 7, wherein the second upper electrode is formed at least two adjacent to the plate line electrode.

9. A semiconductor memory device comprising:

a semiconductor substrate;

a memory transistor formed on the semiconductor substrate, and having first and

second impurity-diffused regions and a gate;

a plug electrode connected to the first impurity-diffused region;

a block selecting transistor formed on the semiconductor substrate and being adjoined to the memory transistor, and having impurity-diffused regions and a gate;

a first wiring connected to the second impurity-diffused region of the memory transistor;

a lower electrode connected to the plug electrode;

a ferroelectric film formed on the lower electrode;

a first upper electrode formed on the ferroelectric film and being connected to the first wiring;

a second upper electrode formed over the gate of the block selecting transistor and being disconnected from the memory transistor, the plug electrode, the block selecting transistor and the first wiring; and

an insulating film formed over the semiconductor substrate, the memory transistor, the plug electrode, the first and second upper electrode, the ferroelectric film and the lower electrode.

10. A semiconductor memory device according to claim 1, wherein a volume of the second upper electrode is less than a volume of the first upper electrode.

11. A semiconductor memory device according to claim 1, wherein the second upper electrode is formed in plural number and is adjacent to the block selecting transistor.

12. A semiconductor memory device according to claim 4, wherein a volume of the second upper electrode is less than a volume of the first upper electrode.

13. A semiconductor memory device according to claim 4, wherein the second upper electrode is formed in plural number and is adjacent to the block selecting transistor.

14. A semiconductor memory device according to claim 6, wherein a volume of the second upper electrode is less than a volume of the first upper electrode.

15. A semiconductor memory device according to claim 6, wherein the second upper electrode is formed in plural number and is adjacent to the block selecting transistor.

16. A semiconductor memory device according to claim 9, wherein a volume of the second upper electrode is less than a volume of the first upper electrode.

17. A semiconductor memory device according to claim 9, wherein the second upper electrode is formed in plural number and is adjacent to the block selecting transistor.

18. A semiconductor memory device comprising:

a semiconductor substrate;

a first memory transistor formed on the semiconductor substrate, and having first and second impurity-diffused regions and a first gate;

a first plug electrode connected to the first impurity-diffused region;

a block selecting transistor formed on the semiconductor substrate and being adjoined to the memory transistor, and having impurity-diffused regions and a second gate;

a first wiring connected to the second impurity-diffused regions of the first memory transistor;

a first lower electrode connected to the first plug electrode;

a first ferroelectric film formed on the lower electrode;

a first upper electrode formed on the first ferroelectric film and being connected to the first wiring;

a second upper electrode formed over the gate of the block selecting transistor and being disconnected from the memory transistor, the first plug electrode, the block selecting transistor and the first wiring;

a second memory transistor formed on the semiconductor substrate, and having third and fourth impurity-diffused regions and a third gate;

a second plug electrode connected to the third impurity-diffused region;

a second lower electrode connected to the second plug electrode;

a second ferroelectric film formed on the second lower electrode;

a second wiring connected to the third impurity-diffused region of the second memory transistor;

a third upper electrode formed on the second ferroelectric film and being connected to the second wiring;

a fourth upper electrode formed over the gate of the second memory transistor and being disconnected from the second memory transistors, the second plug electrode, the block selecting transistor, the first wiring and the second wiring;

an insulating film formed over the semiconductor substrate, the first memory transistor, the second memory transistor, the first plug electrode, the second electrode, the first upper electrode, second upper electrode, the third upper electrode, fourth upper electrode, the first ferroelectric film, the second ferroelectric film, the first lower electrode, and the second lower electrode.

19. A semiconductor memory device according to claim 9, further comprising a second insulating layer formed on the semiconductor substrate, and wherein the second upper electrode is formed in plural number on the second insulating layer.

20. A semiconductor memory device according to claim 18, further comprising a second insulating layer formed on the semiconductor substrate, and wherein the second upper electrode is formed in plural number on the second insulating layer.

21. A semiconductor memory device comprising:

a plurality of memory cells formed on the semiconductor substrate and being connected in series, and respectively having a first impurity-diffused region, a second impurity-diffused region, a gate formed between the first and the second impurity-diffused regions, a plug electrode connected to the first impurity-diffused region, a lower electrode connected to the plug electrode, a ferroelectric layer formed on the lower electrode, a wiring layer connected to the second impurity-diffused region, and an upper electrode connected to the wiring layer;

a block selecting transistor formed adjacent to one end of the plurality of memory cells;

a first conductive layer formed over the block selecting transistor and being separated from the memory cells and the block selecting transistor;

a second conductive layer formed on the first impurity-diffused region and being adjacent to other end of the plurality of memory cells, and being separated from the memory cells; and

a plate line formed over the second conductive layer.

22. A semiconductor memory device according to claim 21, wherein the second conductive layer is provided as two layers adjacent to the plate line.

23. A semiconductor memory device comprising:

a semiconductor substrate;

a memory transistor formed on the semiconductor substrate, and having first and second impurity-diffused regions and a gate;

a plug electrode connected to the first impurity-diffused regions;

a block selecting transistor formed on the semiconductor substrate and being adjoined to the memory transistor, and having impurity-diffused regions and a gate;

a first wiring connected to the second impurity-diffused regions of the memory transistor;

a lower electrode connected to the plug electrode;

a ferroelectric film formed on the lower electrode;

a first upper electrode formed on the ferroelectric film and being connected to the first wiring;

a second upper electrode formed over the gate of the block selecting transistor and the lower electrode, and disconnected from the memory transistor, the plug electrode, the block selecting transistor and the first wiring; and

an insulating layer formed over the semiconductor substrate, the memory transistor, the plug electrode, the first and second upper electrode, the ferroelectric film and the lower electrode.

24. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell block including a plurality of memory transistors formed on the semiconductor substrate, the memory transistors having first and second impurity-diffused regions and a first gate formed between the first and second impurity-diffused regions and being connected in series, a plurality of memory cells connected in series each respectively having a first lower electrode connected to the first impurity-diffused region, a first ferroelectric film formed on the lower electrode and a first upper electrode formed on the first ferroelectric film and being connected to the second impurity-diffused region;

an insulating layer formed on the semiconductor substrate and being adjoined to the first impurity-diffused region of the memory transistor located in one end of the memory cell block;

a block selecting circuit formed on the semiconductor substrate, and being adjoined to the insulating layer, and having a third impurity-diffused region, the fourth impurity diffused region and second gate; and

a first conductive layer formed on the semiconductor substrate, and being connected to the lower electrode of the memory cell located in one end of the merry cell block and the third impurity-diffused region.

25. A semiconductor memory device according to claim 24, wherein the conducting layer have the same material of the lower electrode and is located in a same position as the lower electrode in a vertical direction thereof.

26. A semiconductor memory device according to claim 24, further comprising a second ferroelectric layer formed on the first conductive layer, and a second conductive layer formed on the second ferroelectric layer and being disconnected from the memory cell block, the first conductive layer, the second ferroelectric layer, the third and fourth impurity-diffused regions and the second gate.

27. A semiconductor memory device according to claim 25, further comprising a second ferroelectric layer formed on the first conductive layer, and a second conductive layer formed on the second ferroelectric layer and being disconnected from the memory cell block, the first conductive layer, the second ferroelectric layer, the third and fourth impurity-diffused regions and the second gate.

28. A semiconductor memory device according to claim 24, further comprising a wiring formed over the lower electrode supplying signal to the first gate.

29. A semiconductor memory device according to claim 25, further comprising a wiring formed over the lower electrode supplying signal to the first gate.

30. A method of manufacturing a semiconductor memory, comprising;

forming a transistor including a first impurity-diffused region, a second impurity-diffused region, and a gate between the first impurity-diffused region and the second impurity-diffused region on the semiconductor substrate;

forming a lower electrode layer over the transistor, and being connected to the first impurity-diffused region;

forming a ferroelectric layer on the lower electrode;

forming an upper electrode layer on the ferroelectric layer;

forming the upper electrode layer into a first upper electrode and a second upper electrode;

forming the lower electrode layer and the ferroelectric layer into a capacitor shape;

forming a wiring layer connecting between the first upper electrode and the second impurity-diffused region;

covering the semiconductor substrate, the transistor, the lower electrode, the ferroelectric layer, the wiring layer, the first upper electrode, and the second upper electrode with insulating layer to insulate the second upper electrode from the other except the ferroelectric layer.

31. A manufacturing method of semiconductor memory, comprising;

forming a cell transistor including a first impurity diffused region, a second impurity-diffused region, and a gate between the first impurity-diffused region and the second impurity-diffused region on the semiconductor substrate;

forming a block selecting transistor including a third impurity diffused-region, a fourth impurity-diffused region, and a gate between the third impurity-diffused region and the fourth impurity-diffused region on the semiconductor substrate, and being adjoined to the cell transistor;

forming a lower electrode layer over the cell transistor and the block selecting transistor, and being connected to the first impurity-diffused region;

forming a ferroelectric layer on the lower electrode;

forming an upper electrode layer on the ferroelectric layer;

forming the upper electrode layer into a first upper electrode and a second upper electrode;

forming the lower electrode layer and the ferroelectric layer into a capacitor shape;

forming a wiring layer connecting between the first upper electrode and the second impurity-diffused region; and

covering the semiconductor substrate, the cell transistor, the block selecting transistor, the lower electrode, the ferroelectric layer, the wiring layer, the first upper electrode, and the second upper electrode with insulating layer to insulate the second upper electrode from the other except the ferroelectric layer.